UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,039	06/20/2003	Oliver Chyan	122302.00001	6398

7590 02/11/2005

Michael G. Cameron
Jackson Walker LLP
Suite 600
2435 North Central Expressway
Richardson, TX 75080

EXAMINER	
LE, DUNG ANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/600,039	CHYAN ET AL.	
	Examiner	Art Unit	
	DUNG A LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *11-24,30 and 35-46* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,25-29 and 31-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DLe

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 6/20/03 is acceptable.

Election/Restriction

Application's election without traverse of Group II (Claims 1-10, 25-29, 31-32 and 33-34) in drawn to process of making a semiconductor device is acknowledged for prosecution in the subject application. Applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims.

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 6/20/03 and made of record . The references cited on the PTOL 1449 form have been considered.

Specification

The specification is objected to for the following reason:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed (see MPEP § 606.01).

Note that, the claims are directed to a method of making a semiconductor device instead of to a semiconductor device.

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Omstead et al. (6713373 B1) in view of the following remark.

Omstead et al. teach a method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate 304;

depositing a layer of RuO_2 404 on the inter-level dielectric substrate;

depositing a layer of Ru as a diffusion stuffer on the RuO_2 layer; and

depositing copper on the Ru layer.

Omstead et al. does not teach depositing a layer of Ru on the inter-level dielectric substrate;

depositing a layer of RuO_2 as a diffusion stuffer on the Ru layer; and

depositing copper on the RuO_2 layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made for depositing a layer of Ru on the inter-level dielectric substrate; depositing a layer of RuO_2 as a diffusion stuffer on the Ru layer; and depositing copper on the RuO_2 layer in Omstead et al. 's method, in order to provide an adhesive region on which copper material may be doposited.

Regarding claim 2, further comprising depositing multiple layers of Ru and RuO_2 between the inter-level dielectric substrate and the copper layer (col 2, lines 20-40).

Regarding claim 3,further comprising depositing the RuO.sub.2 layer(s) on the Ru layer(s) using an atomic layer deposition technique (col 3, lines 55-60).

Regarding claim 4, further comprising depositing the RuO.sub.2 layer(s) on the Ru layer(s) using a thermal oxidation technique. (col 3, lines 65- 67).

Regarding claim 5, further comprising depositing the RuO_2 layer(s) on the Ru layer(s) using an electrochemical technique (col 6, lines 25-30).

Regarding claim 6, further comprising depositing the RuO_2 layer(s) on the Ru layer(s) using physical vapor deposition. (col 6, lines 25-30).

Regarding claim 7, further comprising depositing the RuO_2 layer on the Ru layer using an atomic layer deposition technique. (col 6, lines 25- 30)

Regarding claim 8, further comprising depositing the RuO_2 layer on the Ru layer using a thermal oxidation technique. (col 3, lines 65-67)

Regarding claim 9, further comprising depositing the RuO_2 layer on the Ru layer using an electrochemical technique. (col 6, lines 25- 30)

Regarding claim 10, further comprising depositing the RuO_2 layer on the Ru layer using physical vapor deposition. (col 6, lines 25- 30)

Set of claims 25-29

Claims 25- 27 are rejected under 35 USC 102 (e) as being anticipated by Omstead et al. (6713373 B1).

Omstead et al. teaches a method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate 304;

depositing one or a plurality of layers of RuO_2 404 on the inter-level dielectric substrate304; and

depositing copper 604/704 on the RuO_2 layer. (FIGS.7-8, col 25-40)

Regarding claim 26,further comprising depositing the RuO_2 layer on the inter-level dielectric 304 using an atomic layer technique (col 3, lines 55-60).

Regarding claim 27, further comprising depositing the RuO_2 layer on the inter-level dielectric using an electrochemical technique. (col 3, lines 55-60).

Regarding claim 28, further comprising depositing the RuO.sub.2 layer on the inter-level dielectric using a thermal oxidation technique.(col 3, lines 65- 67)

Regarding claim 29, further comprising depositing the RuO_2 layer on the inter-level dielectric using a physical vapor technique. (col 6, lines 25- 30).

Set of claims 31- 32

Claims 31- 32 are rejected under 35 USC 102 (e) as being anticipated by Omstead et al. (6713373 B1).

Omstead et al. teaches a method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ru 408 as a diffusion barrier (Fig. 8,col 5, lines 30-35).

Regarding claim 32, further comprising eliminating a copper seed layer (Fig. 8,col 5, lines 30-35).

Set of claims 33-34

Claims 33-34 are rejected under 35 USC 102 (e) as being anticipated by Omstead et al. (6713373 B1).

Omstead et al. discloses a method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ru 504 and RuO_2 404 as a diffusion barrier 9 (figs. 7- 8).

Regarding claim 34, further comprising eliminating a copper seed layer. (Fig. 8,col 5, lines 30-35).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818